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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,206	06/30/2003	Keith Istvan Farkas	200208214-1	7647

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EXAMINER
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TRAN, VINCENT HUY

ART UNIT	PAPER NUMBER
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2115

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

10/608,206

Applicant(s)

FARKAS ET AL.

Examiner

Vincent T. Tran

Art Unit

2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 21 November 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-16, 18-34, 37-40, 42, 47 and 48 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 33, 34, 37 and 38 is/are allowed.
- 6) ☐ Claim(s) 1-3, 5, 6, 8-16, 18-20, 22-32, 39, 40, 42, 47 and 48 is/are rejected.
- 7) ☒ Claim(s) 4, 7 and 21 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### DETAILED ACTION

1. This Office Action is responsive to the communication filed on 11/21/06
2. Claims 1-16, 18-34, 37-40, 42, 47-48 are pending for examination.
3. The text of those sections of Title 35, U.S. code not included in this action can be found in a prior Office action.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
6. Claims 1, 11-12, 16, 18, 22-24, 47-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazato in view of Fishman U.S. Patent No. 5,017,799 or Owens, Jr. et al. U.S. Patent No. 3,887,842 ("Owens") or Katsukawa U.S. Patent No. 4,653,940.
7. As per claim 1, Nakazato discloses a method of controlling power consumption for at least one computer system, the method comprising:
  - detecting an amount of power consumed by the at least one computer system [0035];
  - comparing the amount of power consumed by the at least one computer system to a threshold [0035, 0039], wherein the threshold is based on the power output of the power supply;
  - and

placing one or more components of the at least one computer system in a lower power state to reduce power consumption in response to the amount of power consumed by the at least one computer system exceeding the threshold [0039].

Although, as discloses by Nakazato in paragraph 0004, 0007, and 0072 in a conventional information processor system, maximum power consumption of the system as a whole is generally estimated during system design. A power supply is used that has a power capacity that allows for the estimated maximum power consumption. With recent general personal computers the power consumption has been increasing as the processing power of CPUs increase. For this reason, a power supply of higher capacity will be required which may result in problems of increased cost, increase size and elevated temperature of the case surface. Therefore, in effort to reduce cost and elevated temperature, a power supply of low power capacity is used where the system power consumption can be reduced with certainty below a set value even in the event that the system is subjected to a heavy load that does not meet the specification of the power supply.

Nakazato does not explicitly teaches the maximum power output of the power supply is based on an average power consumption of the at least one computer system. However, this feature is well know in the art of power supply design.

Fishman teaches another method for reducing the power consumption of loads fed by one or more power supplies is achieved by use of apparatus which determined the power supply output and, upon the occurrence of a predetermined condition, alter the mode of operation so as to reduce the overall demand on the power supply [col. 1 lines 35-62]. Specifically, Fishman teaches, in effort to reduce cost, size, and heat, a smaller capacity power supply is used to provide average power demand capabilities [col. 2 lines 20-27].

Owens teaches another system relates to display systems where the major concern is the significant increase in power consumption with larger, faster and brighter displays [col. 1 lines 25-32]. Specifically, Owens teaches the power supply has been designed with maximum output power equal to the average power requirement of the system. Thus, there is provided a significant reduction in quiescent power, heat generated, and system size and weight [col. 7 lines 5-12].

Katsukawa teaches another apparatus relates to printer. Specifically, Katsukawa teaches conventional printer usually use a power supply of relative small capacity that meets the actual average power consumption, for reduced cost of the power supply [col. 1 lines 25-31].

Therefore, it would have been obvious to one of ordinary skill in the art to have modified the system of Nakazato with the maximum power output of the power supply is based on an average power consumption of the at least one computer system as taught by Nakazato, Owens, Katsukawa since this feature is an old and well know technique in reducing cost, size, and heat in a system.

8. As per claim 11, Nakazato discloses a processor for the at least one computer system is operable to be place in multiple lower power state, each being associated with a lower clock speed, and placing one or ore components of the at least one computer system in a lower power state comprises placing the processor in one of the multiple lower power states [Fig. 4].

9. As per claim 12, Nakazato discloses placing the processor in one or the multiple lower power state comprises instructing the processor not to consume more than a predetermined amount of power [Fig. 4].

10. As per claim 16, Nakazato teaches a system generating power for at least one computer system, the power system comprising:

at least one power supply operable to provide power for the at least one computer system [20-23 fig. 2];

a power monitor operable to determine the power consumption of the at least one computer system [24 fig. 2]; and

a power provisioning system [24 fig. 2, 3] operable to compare the power the power consumption of the at least one computer system to a threshold associated with a maximum capacity of the power supply, and further operable to place one or more components of the at least one computer system in a lower power state in response to the measured power output exceeding the threshold [fig. 4];

Nakazato does not explicitly teaches the maximum capacity of the power supply is based on an average power consumption of the at least one computer system.

Nakazato, Owens, Katsukawa teaches the maximum capacity of the power supply is based on an average power consumption of the at least one computer system [see discussion in claim 1].

11. As per claim 18, see discussion in claim 1.

12. As per claim 22, Nakazato discloses the one or more components comprises a processor, and the power provisioning system is operable to instruct the processor to reduce clock speed for reducing power consumption [fig. 3, 4].

13. As per claim 23, Nakazato discloses the one or more components comprises a processor, and the power provisioning system is operable to instruct the processor to reduce power consumption of the processor to a calculated value or range of value [fig. 4].

14. As per claim 24, Nakazato discloses the one or more components comprise a processor operable to be placed in one of multiple lower power states [fig. 4].

15. As per claim 47, Owens teaches the maximum power output of the power supply is approximately equal to or within a predetermined tolerance of the average power consumption of the at least one computer [see discussion claim 1].

16. As per claim 48, see claim 47.

17. Claims 2-3, 5, 19-20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazato/Owens as applied to claim 1 or 16 above, and further in view of Montero et al.

18. As per claim 2, Nakazato teaches a cooling system is operable to cool the at least one computer system [270 fig. 3]. However, Nakazato does not teach the determining whether

sufficient cooling resource are available and placing at least one component of the at least one computer system in a lower state in response to insufficient cooling resources.

Montero et al. teach another computer system includes a plurality of cooling fans configured to provide sufficient cooling to the system. Specifically, Montero et al. teach determining whether insufficient cooling resources are available for cooling the at least one computer system [paragraph 0028, 0039]; and

placing at least one component of the at least one computer system in lower-power state in response to insufficient cooling resources being available to cool the at least one computer system [paragraph 0045-0046].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the system of Nakazato/Owens with the determining of cooling resources of Montero et al. to placing at least one component of the at least one computer system in a lower state in response to insufficient cooling resources.

The motivation for doing so would have been to prevent damage to the computer system due to insufficient cooling.

Therefore, it would have been obvious to combine Nakazato and Owens with Montero et al. to obtain the invention as specified in claim 2.

19. As per claim 3, Montero et al. teach determine whether excess cooling resources are available for cooling the at least one computer system [From table 3 and paragraph 0046<sup>1</sup>]; and

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<sup>1</sup> the decrease of temperature indicated that excess cooling resources are available.



placing the at least one component of the computer system currently in lower-power state [operating speed at 50%] in a higher-power state [operating speed at 75% inherently at full speed], such that the at least one component consumes more power, in response to excess cooling resources being available.

20. As per claim 5, Montero et al. teach determining whether insufficient cooling resources are available for cooling the at least one computer system comprises determining whether an amount of cooling fluid distributes to the at least one computer system exceeds a threshold associated with the maximum capacity of the cooling system [Table 3 – When both fans are operating and the temperature still increasing up to 96 degree].

21. As per claim 19, Montero et al. teach the power provisioning system is connected to a cooling system [287 fig. 2B] and is operable to receive messages from the cooling system [inherent] associated with the availability of cooling resources for cooling the at least one computer system, the power provisioning system being operable to control the power consumption of the at least one computer system based on a message received from the cooling system [fig. 3].

22. As per claim 20, Montero et al. disclose the power provisioning system is operable to place at least one component of the at least one computer system in a lower-power state in response to receiving a message from the cooling system indicating that insufficient cooling

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resources are available for cooling the at least one computer system [inherently from Table 3 paragraph 0045].

23. Claims 6, 8, 15, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazato/Owens as applied to claim 1 or 16 above, and further in view of Kling et al. (“Kling”).

24. As per claim 6, Nakazato/Owens does not teach comparing the amount of power consumed by the at least one computer system to a second threshold.

Kling teaches another method relates to computer systems and more particularly to limiting the power consumed in computer system by throttling the power consumed by an component in the computer system in response to a high power condition. Specifically, Kling teaches comparing the amount of power consumed by the at least one computer system to a second threshold [paragraph 0035 – total power consumption reaches the lower threshold];

placing the at least one component of the computer system, currently in a lower-power state, in a higher-power state, such that the at least one component consumes more power, in response to the amount of power consumed by the at least one computer system being less than the second threshold [paragraph 0035].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Nakazato/Owens with the second threshold of Kling order to allow the system to resume operation at full speed without damaging the system.

25. As per claim 8, Kling et al. disclose one or more of the threshold based on the maximum power output of the power supply and the second threshold is determined such that a minimal

change in power consumption does not result in changing a power state of the at least one component [paragraph 0033].

26. As per claim 15, Kling et al. disclose placing one or more components in a lower state comprises reducing power consumption of one or more of a processor [paragraph 0031].

27. As per claim 28, see discussion in claim 6.

28. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazato/Owens as applied to claim 1 above, and further in view of Bradley et al..

29. As per claim 9, Nakazato teaches the replacing the at least one component in a lower power state in response to the thermo-coupled in order to cool those computer system. However, Nakazato does not teach placing the at least one component of the at least one computer system in a lower power state in response to the cooling efficiency of the components.

Bradley et al. teach another method for managing power consumption in a computer server. Specifically, Bradley et al. teach determining a cooling efficiency of components in the at least one computer system [42-46 fig. 4]; and

selecting one or more of the components to be placed in a lower power state based on an amount of energy needed to cool the one or more components; wherein a component requiring more energy to be cooled is selected before a component requiring less energy to be cooled [46-47 fig. 4].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Nakazato/Owens with the placing of the at least one component of the at least one computer system in a lower power state in response to the determining of its cooling efficiency as taught by Bradley et al.

The motivation for doing so would have been to provide the system a more efficient way to selectively place the at least one component of the computer system in a lower-power state.

30. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazato/Owens as applied to claim 1 above, and further in view of Oprescu et al.

31. As per claim 13, Nakazato teaches placing one or more components of the at least one computer system in a lower-power state comprises determining the one or more components to be placed in a lower power state base on the priority information. However, Nakazato does not teach expressly the storing of information including components in the at least one computer system, power state of the components, power consumption of the component.

Oprescu et al. teach another power management system that capable of tracking the total amount of power drawn from a bus by devices connected to the bus. Specifically, Oprescu et al. teach a repository [50 fig. 2] storing power state information including power consumption and priority information, wherein the power provisioning system is operable to utilize the power state information to identify a component of the one or more components [col. 8 lines 43-51] to be placed in a lower-power state or a higher power state [109, 114, 115 – 110 fig. 2].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Nakazato/Owens with the repository storing power

state information as taught by Oprescu et al. in order to provide the power controller the ability to precisely determining the actual power requirements of devices and more effectively controlling the operation of the devices to efficiently utilize available power [col. 3 lines 1-14].

32. As per claim 14, Nakazato teaches placing the at least one component of the computer system currently in a lower power state in a higher power state. However, Nakazato system modified by Oehler et al. do not teach placing the component in to a higher power state based on the stored information. However, it would have been obvious to one of ordinary skill in the art that, since the system placing a component into the lower power state base on the stored information, the system would included the claimed placing of a component into the higher power state based on the stored information.

33. Claims 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazato/Owens as applied to claim 16 above, and further in view of Oprescu et al.

34. As per claim 26, Nakazato teaches the power control, when the amount of power consumed by the at least one computer system exceeded a threshold, selectively powering off lower priority devices to reduce the power drawn. However, Nakazato does not teach a repository storing power state information for the one or more of components in the at least one computer system, wherein the power provisioning system is operable to utilize the power state information to identify a component of the one or more components to be placed in a lower-power state or a higher power state.

Oprescu et al. teach another power management system that capable of tracking the total amount of power drawn from a bus by devices connected to the bus. Specifically, Oprescu et al. teach a repository [50 fig. 2] storing power state information, wherein the power provisioning system is operable to utilize the power state information to identify a component of the one or more components [col. 8 lines 43-51] to be placed in a lower-power state or a higher power state [109, 114, 115 – 110 fig. 2].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Nakazato/Owens with the repository storing power state information as taught by Oprescu et al. in order to provide the power controller the ability to precisely determining the actual power requirements of devices and more effectively controlling the operation of the devices to efficiently utilize available power [col. 3 lines 1-14].

35. As per claim 27, Oprescu et al. teach the power state information comprises one or more of power consumption of the one or more components and priority information associated with prioritizing the one or more components for changing the power state of the one or more components [50 fig. 2].

36. Claims 39-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazato/Owens in view of Montero et al.

37. As per claim 39, Nakazato discloses an apparatus controlling power consumption of at least one computer system using a power supply means, the apparatus comprising:

means for determining an amount of power consumed by the at least one computer system [24 fig. 2];

means for comparing the amount of power to a threshold, wherein the threshold is based on the power output of the power supply means; and

means for placing one or more components of the at least one computer system in a lower power state to reduce power consumption in response to the power consumption of the at least one computer system exceeding the threshold [fig. 4]; and

Owens teaches the power supply means has a maximum power output based on an average power consumption of the at least one computer system [see discussion in claim 1].

Nakazato/Owens does not teach means for cooling is further operable to determine whether excess cooling resources are available for cooling the at least one computer system.

Montero et al. teach another computer system includes a plurality of cooling fans configured to provide sufficient cooling to the system. Specifically, Montero et al. teach means for cooling is further operable to determine whether excess cooling resources are available for cooling the at least one computer system; and

the means for placing the at least one component [CPU] of the computer system currently in a lower state is further inherently operable to place the at least one component in a higher power state such that the at least one component consumes more power, in response to excess cooling resources being available [table 3 of paragraph 0045; 0046; see further discussion in claim 3].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Nakazato/Owens with the means to determine

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whether excess cooling resources are available for cooling the at least one computer system of Montero et al. to place the at least one component [CPU] of the computer system currently in a lower state is further operable to place the at least one component in a higher power state such that the at least one component consumes more power, in response to excess cooling resources being available

38. As per claim 40, see discussion in claim 2.

39. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazato/Owens and Montero et al. as applied to claim 39 above, and further in view of Kling.

40. As per claim 42, see discussion in claim 6.

41. Claims 1, 10, 16, 25, 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bodas in view of Fishman or Owens or Katsukawa.

42. As per claim 1, Bodas discloses a method of controlling power consumption for at least one computer system, the method comprising:

detecting an amount of power consumed by the at least one computer system [paragraph 0028];

comparing the amount of power consumed by the at least one computer system to a threshold [step 605 fig. 6], wherein the threshold is based on the power output of the power supply [paragraph 0005-0007, 0023, 0033]; and



place one or more components of the at least one computer system in a lower power state to reduce power consumption in response to the amount of power consumed by the at least one computer system exceeding the threshold [step 620 fig. 6; paragraph 0029].

Bodas further teaches a computer system typically provides power supply which may have a maximum output that is higher than the estimated power consumption, resulting in unnecessary demand on the supporting infrastructure including, for example, unnecessary computer racks, cooling capacity, and expensive. Thus, by setting the target power consumption level to an average power consumption of the system, the system may allow for better utilization and improved efficiency of the supporting infrastructure including, for example, available power and cooling capacity. Bodas does not explicitly teaches the maximum output of the power supply is based on an average power consumption of the at least one computer system.

However, this feature is well know in the art of estimate power supply requirement of a system as disclosed by Fishman, Owens, and Katsukawa.

Fishman teaches another method for reducing the power consumption of loads fed by one or more power supplies is achieved by use of apparatus which determined the power supply output and, upon the occurrence of a predetermined condition, alter the mode of operation so as to reduce the overall demand on the power supply [col. 1 lines 35-62]. Specifically, Fishman teaches, in effort to reduce cost, size, and heat, a smaller capacity power supply is used to provide average power demand capabilities [col. 2 lines 20-27].

Owens teaches another system relates to display systems where the major concern is the significant increase in power consumption with larger, faster and brighter displays [col. 1 lines 25-32]. Specifically, Owens teaches the power supply has been designed with maximum output

power equal to the average power requirement of the system. Thus, there is provided a significant reduction in quiescent power, heat generated, and system size and weight [col. 7 lines 5-12].

Katsukawa teaches another apparatus relates to printer. Specifically, Katsukawa teaches conventional printer usually use a power supply of relative small capacity that meets the actual average power consumption, for reduced cost of the power supply.

Therefore, it would have been obvious to one of ordinary skill in the art to have modified the system of Bodas with the maximum power output of the power supply is based on an average power consumption of the at least one computer system as taught by Nakazato, Owens, Katsukawa since this feature is an old and well know technique in reducing cost, size, and heat in a system.

43. As per claim 10, Bodas discloses the prioritizing applications running on the multiple computer systems; wherein

the step of placing one or more components in a lower power state further comprises identifying one of the multiple computer systems running one or more low priority applications, and placing at least one component in the identified computer system in a lower power state [paragraph 0036].

44. As per claim 16, Bodas discloses a system generating power for at least one computer system, the power system comprising:

at least one power supply operable to provide power for the at least one computer system [240 fig. 2];

a power monitor operable to determine the power consumption of the at least one computer system [205 fig. 2]; and

a power provisioning system [250 fig. 2, 3] operable to compare the power the power consumption of the at least one computer system to a threshold associated with a maximum capacity of the power supply, and further operable to place one or more components of the at least one computer system in a lower power state in response to the measured power output exceeding the threshold [step 605 fig. 6]; and

Owens teaches the maximum capacity of the power supply is based on an average power consumption of the at least one computer system [see discussion in claim 1].

45. As per claim 25, Bodas discloses the at least one computer system comprises multiple computer systems [fig. 3], and the power provisioning system is operable to prioritize the multiple computer systems for placement in lower-power state based on an importance of applications executing on the multiple computer systems [paragraph 0036].

46. As per claim 29, Bodas discloses the at least one computer system comprises multiple computer systems receiving power via a power bus, and the power provisioning is operable to disconnect a portion of a power bus to place one of the multiple computer in a lower power state [inherent fig. 2].

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47. As per claim 30, Bodas. discloses the power monitor [205 fig. 2] is connected to the at least one power supply [204 fig. 1] to measure the output power of the at least one power supply for determining the power consumption of the at least one computer system [paragraph 0042].

48. As per claim 31, Bodas discloses the at least one computer system comprises multiple computer systems connected to the at least one power supply via a power bus [inherent fig. 2 and 3], and the power monitor is connected to the power bus to measure the power consumption of the multiple computer systems [paragraph 0033-0034].

49. As per claim 32, Bodas discloses the one or more components comprise one or more of a processor, a floating point unit, one or more storage devices, one or more memory ICs, and a cache or a portion of a cache [inherent].

***Allowable Subject Matter***

50. Claim 33-34, 37, 38 allowed.

51. Claims 4, 7, 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

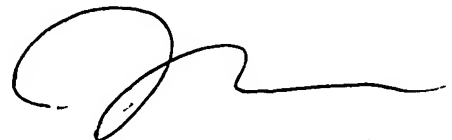
***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Tran

A handwritten signature in black ink, consisting of a large, stylized 'V' followed by a horizontal line that tapers off to the right.